

# Deep Learning Hardware Acceleration University Of Toronto

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### Deep Learning Hardware Acceleration University

#### **Deep Learning Hardware Acceleration - University of Toronto**

Deep Learning Hardware Acceleration Jorge Albericio+ Alberto Delmas Lascorz Patrick Judd Sayeh Sharify Tayler Hetherington\* Natalie Enright Jerger Tor Aamodt\*

#### **VTA: An Open Hardware-Software Stack for Deep Learning**

VTA: An Open Hardware-Software Stack for Deep Learning Thierry Moreau, Tianqi Chen, Ziheng Jiang, Luis Ceze, Carlos Guestrin, Arvind Krishnamurthy Paul G Allen School of Computer Science & Engineering, University of Washington Abstract Hardware acceleration is an enabler for ubiquitous and efficient deep learning With hardware accelerators being

#### **Value-Based Deep-Learning Acceleration**

Value-Based Deep-Learning Acceleration This article summarizes our recent work on value-based hardware accelerators for image classification using Deep Convolutional Neural Networks (CNNs) The presented designs exploit runtime value properties that are difficult or impossible to discern in advance These include values that are zero or near

#### **1 A Hardware-Software Blueprint for Flexible Deep Learning ...**

1 A Hardware-Software Blueprint for Flexible Deep Learning Specialization Thierry Moreau 1, Tianqi Chen , Luis Vega 1, Jared Roesch , Eddie Yan , Lianmin Zheng2, Josh Fromm , Ziheng Jiang1, Luis Ceze 1, Carlos Guestrin , Arvind Krishnamurthy1 1Paul G Allen School of Computer Science & Engineering, University of Washington 2Shanghai Jiao Tong University F

#### **DATA ANALYTICS USING DEEP LEARNING - cc.gatech.edu**

•What is hardware acceleration? •If you use any non-CPU hardware that can speed up your program, that is hardware acceleration Examples: 6

Applications Hardware accelerator Computer graphics GPUs are good with 'some' operations but can have thousands of cores in a single GPU  
Enables parallel processing GPUs need CPU to control them

### **Hardware Acceleration of Deep Convolutional Neural ...**

ing opportunities for speci c acceleration hardware, eg FPGA, by customizing the digital circuit speci c for the deep learning algorithm inference  
However, deploy-ing CNNs on portable and embedded systems is still challenging due to large data volume, intensive computation, varying algorithm structures, and frequent memory accesses

### **Towards Ultra-High Performance and Energy Efficiency of ...**

Towards Ultra-High Performance and Energy Efficiency of Deep Learning Systems: An Algorithm-Hardware Co-Optimization Framework Yanzhi Wang<sup>1</sup>, Caiwen Ding<sup>1</sup>, Zhe Li<sup>1</sup>, Geng Yuan<sup>1</sup>, Siyu Liao<sup>2</sup>, Xiaolong Ma<sup>1</sup>, Bo Yuan<sup>2</sup>, Xuehai Qian<sup>3</sup>, Jian Tang<sup>1</sup>, Qinru Qiu<sup>1</sup>, Xue Lin<sup>4</sup> <sup>1</sup>Department of Electrical Engineering and Computer Science, Syracuse University, Syracuse, NY 13244

### **TOWARDS EFFICIENT HARDWARE ACCELERATION OF DEEP ...**

TOWARDS EFFICIENT HARDWARE ACCELERATION OF DEEP NEURAL NETWORKS ON FPGA by Sicheng Li MS in Electrical Engineering, New York University, 2013 BS in Electrical Engineering, Beijing University of Posts and Communications, 2011 Submitted to the Graduate Faculty of the Swanson School of Engineering in partial fulfillment

### **DI HARDWARE ACCELERATION OF DEEP LEARNING RESULTS ...**

their hardware accelerators HARDWARE ACCELERATION OF DEEP LEARNING Allocation: Illinois/50 Knh PI: Tao Xie<sup>1</sup> Co-PI: Yuan Xie<sup>2</sup> <sup>1</sup>University of Illinois at Urbana-Champaign <sup>2</sup>University of California, Santa Barbara EXECUTIVE SUMMARY Our project aims to use the Blue Waters platform for hardware acceleration of deep learning for big data image

### **Accelerating Binarized Convolutional Neural Networks with ...**

fer further automation features for generating the hardware-software interface and on-chip memory network In the con-text of deep learning, these tools have the potential to criti-cally reduce time-to-market on new accelerator designs and thus reduce the aforementioned innovation gap In this paper we present the design of a BNN accelerator

### **EFFICIENT METHODS AND HARDWARE FOR DEEP LEARNING ...**

EFFICIENT METHODS AND HARDWARE FOR DEEP LEARNING A DISSERTATION Approved for the Stanford University Committee on Graduate Studies Patricia J Gumport, Vice Provost for Graduate Education the efficient acceleration on general-purpose ...

### **From Model to FPGA: Software-Hardware Co-Design for ...**

From Model to FPGA: Software-Hardware Co-Design for Efficient Neural Network Acceleration Kaiyuan Guo<sup>1,2</sup>, Lingzhi Sui<sup>1</sup>, Jiantao Qiu<sup>2</sup>, Song Yao<sup>1</sup>, Song Han<sup>1,3</sup>, Yu Wang<sup>1,2</sup>, Huazhong Yang<sup>1</sup> <sup>1</sup> DeePhi Technology <sup>2</sup> Tsinghua University, <sup>3</sup> Stanford University Acknowledgement: Dongliang Xie and DeePhi Engineering Team

### **Deep Learning on FPGAs - University of Guelph**

DEEP LEARNING ON FPGAS Gri n James Lacey Advisor: University of Guelph, 2016 Dr Graham W Taylor Co-Advisor: Dr Shawki Areibi The recent successes of deep learning are largely attributed to the advancement of hardware acceleration technologies, which can accommodate the incredible growth of data sizes and model complexity The

### **HyPar: Towards Hybrid Parallelism for Deep Learning ...**

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importance of deep learning, we argue that DNN training acceleration is a crucial problem. Currently, DNNs are typically trained by high-performance computer systems with high-end CPUs/GPUs, which are not performance and energy efficient. While many accelerators focused on acceleration for DNN inference, training was only considered in a few

### **SOFTWARE-HARDWARE CODESIGN FOR EFFICIENT NEURAL NETWORK ...**

software-hardware codesign for efficient neural network acceleration. Designers making deep learning computing more efficient cannot rely solely on hardware. Incorporating software-optimization techniques such as model compression leads to significant power savings and performance improvement. This article provides an overview of DeepPhi's technology flow,